ABSTRACT OF THE DISCLOSURE

A microprocessor that can prevent the generation of the branch penalty even when a branch prediction is not hit, thereby improving the processing efficiency, and achieving low power consumption. The microprocessor employs a limited conditional branch instruction whose instruction to be executed next when the branch prediction is not hit is limited. The microprocessor includes a memory for storing instructions and a dedicated register for storing an op code of the limited instruction. When it is detected that the branch prediction is not hit by decoding the limited conditional branch instruction, the op code of the instruction to be executed next is provided from the dedicated register to the decoder and the operand of the instruction to be executed next is provided from the memory to the decoder. The decoder can start the decode operation because the op code is provided from the dedicated register in a short period, so the decode operation can be conducted within few machine cycles, the branch penalty generation can be prevented, and the processing efficiency is improved and low power consumption is achieved.